AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of listings of claims in the application.

1. (Currently amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region defined thereon;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate having at least a substantial portion thereof disposed over said channel region and separated therefrom by said fist insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a first portion of said top surface of said floating gate and being separated from said floating gate by said second insulating layer, said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a second portion of said top surface of said floating gate and being separated from said second one of said side walls and said portion of said top surface of said floating gate by said second insulating layer;

a drain region formed in a portion of said substrate proximate said first portion of the control gate; and

a source region formed in a portion of said substrate proximate said erase gate, said source region having a substantial portion thereof underneath said floating

gate;

wherein during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

2. (Previously presented) A semiconductor device having at least one transistor as recited in claim 1, wherein said erase gate overlaps said floating gate and at least a portion of said control gate.

G1 (cont'd)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Currently amended) A memory array disposed on a substrate comprising a plurality of memory cells each having a channel region formed in said substrate, a floating gate separated from said channel region by a first insulating layer, an erase gate, a control gate separated from said floating gate by a second insulating layer, a source region, and a drain region, comprising:
a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same row are connected by a common erase line, the source regions of the memory cells in the same rows are connected by a common source line, and the drain regions of memory cells in the

same columns are commonly connected via a common drain line, wherein at least a portion of each said control gate is disposed over a portion of said channel region and is separated therefrom by said second insulating layer, said portion of the control gate being proximate to said drain region, and wherein a portion of said control gate is disposed in facing relationship to a side surface of said floating gate and is separated therefrom by said second insulating layer; and

a control circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array;

wherein said source region having a substantial portion thereof underneath said floating gate, and wherein during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

9. (Previously presented) A memory array disposed on a substrate as recited in claim 8 wherein said floating gate has a least a substantial portion thereof disposed over said channel region and is separated therefrom by said first insulating layer, said control gate is substantially placed on one side of said floating gate and separated therefrom by said second insulation layer, said erase gate is substantially placed on a second side of said floating gate and is separated therefrom by said second insulation layer, said drain region is substantially disposed on said on side of said floating gate, and said source region is substantially disposed on said second side of said floating gate.

10. (Previously presented) A memory array as recited in claim 9, wherein said erase gate overlaps said floating gate and at least a portion of said control gate.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

G' (cntd)

16. (Currently amended) A semiconductor device having at least one transistor, the device comprising:
a substrate having a channel region;
a first insulating layer disposed over said channel region and over at least a portion of said substrate;
a floating gate having at least a substantial portion thereof disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;
a second insulating layer disposed over said side walls and over said top surface of said floating gate;
a control gate having a first portion disposed over a first portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first one of said side walls;
an erase gate formed over a second one of said side walls and over at least a second portion of said top surface of said floating gate and being separated from said second one of said side walls and said portion of said top surface of said floating gate by said second insulation layer;

a source region formed in a portion of said substrate proximate said erase gate; and a drain region formed in a portion of said substrate proximate said first portion of the control gate.~~;~~

~~wherein during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.~~

G' (cntd)

17. (Previously presented) A semiconductor device having at least one transistor as recited in claim 16 wherein said erase gate is disposed over at least a portion of each of said floating gate and said control gate.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Currently amended) A memory array disposed on a substrate comprising a plurality of memory cells each having a channel region formed in said substrate, a floating gate separated from said channel region by a first insulating layer, an erase gate, a control gate separated from said floating gate by a second insulating layer, a source region, and a drain region, comprising:
a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same row are connected by a

common erase line, the source regions of the memory cells in the same rows are connected by a common source line, and the drain regions of memory cells in the same columns are commonly connected via a common drain line, wherein at least a portion of each said control gate is disposed over a portion of said channel region and is separated therefrom by said second insulating layer, said portion of the control gate being proximate to said drain region, ~~said portion of said channel region being proximate said drain region,~~ and wherein a portion of said control gate is disposed in facing relationship to a side surface of said floating gate and is separated therefrom by said second insulating layer; and

G' (cntd)

a control circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array.

24. (Previously presented) A memory array disposed on a substrate as recited in claim 23 wherein said floating gate has a least a substantial portion thereof disposed over said channel region and is separated therefrom by said first insulating layer, said control gate is substantially placed on one side of said floating gate and separated therefrom by said second insulation layer, said erase gate is substantially placed on a second side of said floating gate and is separated therefrom by said second insulation layer, said drain region is substantially disposed on said on side of said floating gate, and said source region is substantially disposed on said second side of said floating gate.

25. (Previously presented) A memory array as recited in claim 24, wherein said erase gate overlaps said floating gate and at least a portion of said control gate